COMPUTER SCIENCE

HfZrO-based synaptic resistor circuit for a Super-Turing intelligent system

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Computers based on the Turing model execute artificial intelligence (AI) algorithms that are either programmed by humans or derived from machine learning. These AI algorithms cannot be modified during the operation process according to environmental changes, resulting in significantly poorer adaptability to new environments, longer learning latency, and higher power consumption compared to the human brain. In contrast, neurobiological circuits can function while simultaneously adapting to changing conditions. Here, we present a brain-inspired Super-Turing AI model based on a synaptic resistor circuit, capable of concurrent real-time inference and learning. Without any prior learning, a circuit of synaptic resistors integrating ferroelectric HfZrO materials was demonstrated to navigate a drone toward a target position while avoiding obstacles in a simulated environment, exhibiting significantly superior learning speed, performance, power consumption, and adaptability compared to computer-based artificial neural networks. Synaptic resistor circuits enable efficient and adaptive Super-Turing AI systems in uncertain and dynamic real-world environments.

INTRODUCTION

The development of artificial intelligence (AI) systems has predominantly relied on computers. Following the Turing model (*1*), computers can accurately execute predetermined inference algorithms programmed by humans and/or derived from machine learning processes (*2*–*11*). Present neuromorphic computing circuits, using digital electronics (*4*–*7*) or analog resistive devices such as floating-gate transistors (*12*–*14*), memristors (*15*–*19*), ferroelectric junctions (*20*) and diodes (*21*), and phase-change memory resistors (*22*), can execute inference algorithms previously programmed through learning (training). All computing circuits can only execute algorithms that are explicitly predefined, and these algorithms remain fixed and cannot be modified during the computing processes in response to environmental changes. AI systems need to improve their ability to handle diverse and complex conditions by expanding their prelearning domains through the use of "big data," which significantly increases the time and energy required for learning (*2*–*11*). Consequently, the computationally intensive learning processes are often carried out on large-scale, power-hungry off-site computers to derive optimal inference algorithms, which are then executed on edge computers with a stringent power budget. With their accurate execution of the predefined inference algorithms, AI systems, such as self-driving cars (*8*), drones (*9*, *10*), robotic systems (*23*), and large language models (*11*), may outperform humans within their learning domains. However, these AI systems lack the adaptability of the human brain and are prone to failure in unknown environments that extend beyond their learning domains (*8*–*11*, *23*). For example, accidents occurred when self-driving cars operated in environments beyond their prelearned domains (*8*). Navigating a self-driving drone in unpredictable, complex environments, such as those with obstacles and strong winds, incurs complex turbulence, instability, and collisions, making it one of the most significant challenges in the development of self-driving aerial vehicles (*10*). Attempting to expand learning domains through the utilization of even more data through the utilization of "big data" from complex changing environments is expensive, inefficient, and unsustainable (*24*, *25*), and the inference algorithms derived from finite learning domains restrict their performance in real-world environments with infinite variations.

The brain has long inspired the development of AI technology. Neurobiological networks in the brain process massive spike signals input to presynaptic neurons, generating currents through synapses and triggering output spikes at postsynaptic neurons in analog parallel mode (*26*–*30*). Human brains can perform algorithmic computations in Turing mode, following prelearned algorithms that remain fixed during the computations (*31*–*33*). However, the brain can also process information without predefined algorithms by learning in real time; its synaptic connections can be modified while performing a task (*26*, *28*, *30*), referred to as Super-Turing computing (*31*–*33*). In neurobiological circuits, synaptic weights (conductance) can be modified during concurrent inference and learning processes by following a learning rule known as spike timing–dependent plasticity (STDP) (Materials and Methods) (*28*, *30*). The ability to simultaneously infer and learn sets the brain apart from computers, leading to significantly shorter learning latency and greater adaptability to dynamically changing environments compared to computers (*34*). The brain often computes based on previously learned experiences but switches to a Super-Turing mode when encountering unexpected conditions that require new learning and adaptation (*32*). For instance, self-driving cars can operate within their prelearned domains, but when they encounter new conditions, human drivers

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must intervene, devising solutions using their concurrent inference and learning abilities. Although the Super-Turing computing models have been postulated theoretically (*31*, *32*), they did not address the concurrent inference and learning functionality of neurobiological circuits. Experimentally, neuromorphic computing circuits based on either digital transistors (*4*–*7*) or analog resistive devices (*12*–*22*) have been typically operated in the Turing computing mode with sequential learning and inference processes. Various learning algorithms, such as STDP, have been successfully implemented in the circuits of analog resistive devices by applying specific "learning" signals to modify the device conductance; the inference algorithm must be executed sequentially, rather than concurrently, by applying different signals to prevent changes in the device conductance (*12*, *13*, *15*–*19*, *22*). For instance, the memristor conductance was modified according to the STDP learning rule by applying voltage pulses with amplitudes of ±1.7 V, whereas the conductance was read out by applying voltage pulses with an amplitude of 0.4 V to prevent changes in the device conductance (*16*). In previously reported two-terminal ferroelectric tunnel junctions (*20*) and ferroelectric diodes (*21*), device conductance could be tuned for learning with high-magnitude voltages, whereas low-magnitude voltages were used for reading or inference to avoid altering conductance. They cannot perform learning and inference simultaneously. The existing neuromorphic circuits still operated in the Turing mode, and the inference algorithm executed in these circuits cannot be adjusted for learning during inference. The key for Super-Turing computing is to be able to adjust weights in real time during inference. How can we emulate concurrent learning and inference in an electronic system?

In this study, we initially introduce a model of an intelligent system based on a synaptic resistor (synstor) circuit (*35*–*37*) with the concurrent inference and learning functionality, operating in parallel analog Super-Turing mode. We fabricated a circuit of $Hf_{0.5}Zr_{0.5}O_2$-based synstors to implement the concurrent inference and learning. We conducted experiments to navigate an aerial drone toward a target position by avoiding obstacles using the synstor circuit and human operators and a computer-based artificial neural network (ANN), in a simulated aerodynamic environment with time-varying strong winds. The experimental results demonstrated that the synstor circuit and human operators significantly outperformed the ANN in terms of learning speed, performance, power consumption, and adaptability to the changing environment.

RESULTS

Super-Turing intelligent system based on a synstor circuit

Similar to a neurobiological network connected by synapses, a circuit composed of M input and N output electrodes connected by $M \times N$ synstors is depicted in Fig. 1A. Voltage pulses ($\mathbf{x}$) applied at the input electrodes induce currents ($\mathbf{I}$) through the synstors at the output electrodes to execute an inference function

$$\mathbf{I} = \mathbf{W}(t)\,\mathbf{x} \tag{1}$$

where $\mathbf{W}(t)$ denotes the conductance matrix of the synstors. The excitatory (or inhibitory) currents ($\mathbf{I}$) trigger (or inhibit) the voltage pulses ($\mathbf{y}$) applied on actuators via neuron and interface circuits to modify the states of a system ($\mathbf{s}$). The deviations of $\mathbf{s}$ from targeted states $\hat{\mathbf{s}}$, denoted as $\mathbf{s} - \hat{\mathbf{s}}$, are detected by sensors and converted to $\mathbf{x}$ by interface circuits (Fig. 1B). The aim is to minimize the objective function $F = \frac{1}{2}(\mathbf{s} - \hat{\mathbf{s}})^2$, tuning $\mathbf{s}$ toward $\hat{\mathbf{s}}$.

Unlike standard ANNs, where the weights remain unchanged during the execution of their inference functions, the $\mathbf{W}(t)$ in the synstor circuit, similar to a neurobiological network, may be modified during the inference process by following a correlative learning rule (*26*, *28*, *30*)

$$\frac{d\mathbf{W}}{dt} = \alpha\,\mathbf{z}(t) \otimes \mathbf{x}(t) \tag{2}$$

where α denotes a learning coefficient, $\mathbf{z}$ denotes voltage pulses triggered at the output electrodes of the circuit, and $\mathbf{z}(t) \otimes \mathbf{x}(t)$ represents the outer product between $\mathbf{z}(t)$ and $\mathbf{x}(t)$. The STDP learning rule (*28*, *30*) can also be formulated as Eq. 2, where the temporal mean $\overline{z} = 0$ (Materials and Methods and Eq. 3) and the temporal covariance between z_n and y_n, $\overline{z_n y_n} \leq 0$ (Materials and Methods and

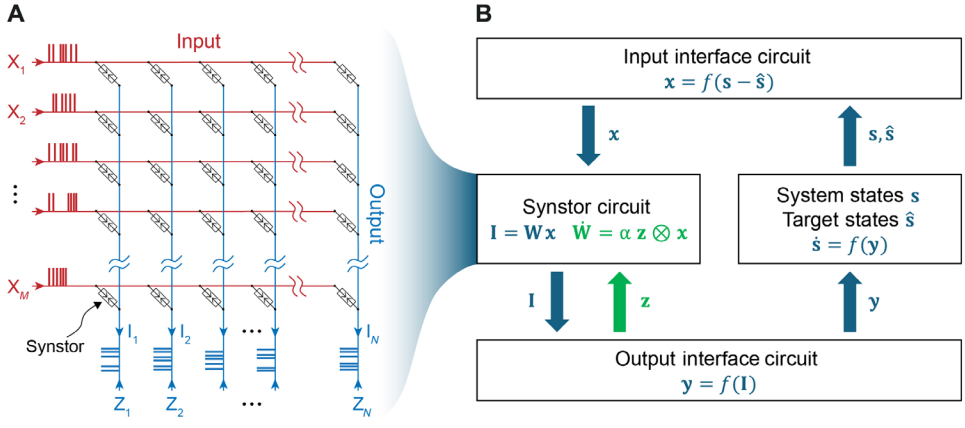

Fig. 1. Synstor circuit for intelligent systems. (**A**) Schematic diagram showing a crossbar synstor circuit composed of $M \times N$ synstors connected with M input electrodes and N output electrodes. $\mathbf{x}$ denotes a vector with element x_m as the voltage pulses applied to the mth input electrode, $\mathbf{z}$ denotes a vector with element z_n as the voltage pulses applied to the nth output electrode, and $\mathbf{I}$ denotes a vector with element I_n as the current induced at the nth output electrode. (**B**) Sensors detect deviations of the states of a system ($\mathbf{s}$) from targeted states ($\hat{\mathbf{s}}$), denoted as $\mathbf{s} - \hat{\mathbf{s}}$, and convert them to input voltage pulses ($\mathbf{x}$) using an interface circuit. The output currents, $\mathbf{I} = \mathbf{W}\mathbf{x}$, triggered by $\mathbf{x}$ from the synstor circuit flow into an output interface circuit, generating output voltage pulses ($\mathbf{y}$) applied on actuators to modify $\mathbf{s}$, as well as voltage pulses ($\mathbf{z}$) applied on the output electrodes of the synstor circuit to modify the synstor conductance matrix ($\mathbf{W}$) according to the learning rule $\dot{\mathbf{W}} = \alpha\,\mathbf{z} \otimes \mathbf{x}$.

Eq. 4). When $\mathbf{z}$ in Eq. 2 satisfies the conditions $\overline{\mathbf{z}} = 0$ and $\overline{z_n y_n} \leq 0$, the concurrent execution of the inference (Eq. 1) and learning (Eq. 2) in the synstor circuit results in the decrease in the objective function F [i.e., $\overline{\left(\frac{dF}{dt}\right)} \leq 0$; Materials and Methods and Eq. 5]. When $\overline{\left(\frac{dF}{dt}\right)} < 0$, $\mathbf{W}$ deviates from $\widehat{\mathbf{W}}$ due to environmental, system, or circuit changes, and $\mathbf{W}$ is adjusted toward $\widehat{\mathbf{W}}$ to decrease $\overline{F}$ during concurrent learning and inference processes. In this case, the circuit operates in Super-Turing mode. When the covariance between $\mathbf{z}$ and $\mathbf{x}$, $\overline{\mathbf{z} \otimes \mathbf{x}} = 0$, then $\overline{\frac{d\mathbf{W}}{dt}} = 0$, $\overline{\left(\frac{dF}{dt}\right)} = 0$, and $\mathbf{W} = \widehat{\mathbf{W}} = arg\min_{\mathbf{W}} F$ remain unchanged during the execution of the inference function, $\mathbf{I} = \widehat{\mathbf{W}}\mathbf{x}$, and the circuit operates in the Turing mode. To execute the correlative learning rule ($\dot{\mathbf{W}} = \alpha\, \mathbf{z} \otimes \mathbf{x}$) by applying various $\mathbf{z}$ pulses, different learning functions in all three major machine learning paradigms (unsupervised, supervised, and reinforcement learning) can be implemented in multilayer synstor circuits (*29*).

Synstor circuit based on HfZrO ferroelectric materials

The synstor circuit poses a challenging demand for materials and devices that can facilitate the precise, reliable, fast, and repetitive execution of both analog inference and learning concurrently. In this work, we fabricated synstors by integrating a $WO_{2.8}/Hf_{0.5}Zr_{0.5}O_2$ heterojunction with a Si channel in each device. Hf oxides have emerged as promising ferroelectric materials, enabling scalable, Si-compatible nonvolatile analog memory and neuromorphic devices (*38*–*42*). As shown in Fig. 2A, a crossbar synstor circuit was fabricated by following the process described in Materials and Methods and illustrated in fig. S1. The structure and materials of the synstors were characterized by scanning transmission electron microscopy (STEM), energy-dispersive x-ray (EDX) spectroscopy, and electron energy loss spectroscopy (EELS) and are shown in Fig. 2 (B to D), and fig. S2. A 40-μm-long 220-nm-thick Si channel with a boron doping concentration of 10^{15} / cm^3 was made from a single-crystal Si layer on a 3-μm-thick SiO_2 layer. A 14-μm-long 80-nm-thick $WO_{2.8}$ reference electrode was fabricated on a 12.6-nm-thick $Hf_{0.5}Zr_{0.5}O_2$ layer on a 3.5-nm-thick SiO_2 dielectric layer on the Si channel. The $Hf_{0.5}Zr_{0.5}O_2$ layer was composed of ferroelectric orthorhombic, dielectric tetragonal and monoclinic phases (*40*). A 12-nm-thick metallic $TiSi_{0.9}$ layer was sandwiched between the Ti input/output electrodes and Si channel and formed a Schottky contact to the Si channel (*43*).

To emulate synapses grounded to the cerebrospinal fluid in neurobiological circuits, the reference electrodes of synstors were always grounded during the tests. When voltage pulses with an amplitude x were applied on a synstor in the circuit to induce current I through the synstor, a nonlinear $I - x$ relation (Fig. 3A) revealed the Schottky barriers between the Si channel and $TiSi_{0.9}$ layers (*43*). The synstor circuit executes the inference function $\mathbf{I} = \mathbf{W}\mathbf{x}$ (Eq. 1), when multiple voltage pulses, $\mathbf{x}$, are applied on the input electrodes. The learning functionality of synstors was tested by the application of x and z pulses with various amplitudes, numbers, and widths on their input and output electrodes, respectively. After a synstor experienced 690 paired x and z pulses with amplitudes $x = z$ and a width of 2 ms, the percentage changes in w, $(\Delta w/w_0) \times 100\%$, increased from 0 to 102% when the voltage amplitudes increased from 1.2 to 3 V; $\Delta w / w_0$ decreased from 0 to −95% when x and z decreased from −1.2 to −3 V; when the voltage amplitudes $-1.2\ \text{V} \leq x = z \leq 1.2\ \text{V}$, $|\Delta w / w_0| \approx 0$ (Fig. 3B). The synstor conductance was gradually tuned in analog mode by applying individual paired pulses with amplitudes $x = z = \pm 3$ V and a width of 2 ms (Fig. 3C). After the synstor experienced x or z pulses with $-3\ \text{V} \leq x \leq 3\ \text{V}$ and $z = 0$ V, or $x = 0$ V and $-3\ \text{V} \leq z \leq 3\ \text{V}$, $|\Delta w / w_0| \approx 0$ (Fig. 3, B and C). Synstors in the circuit executed the learning function, $\dot{w}_{nm} = \alpha\, z_n\, x_m$ (Eq. 2) with the modification coefficient $\alpha \geq 0$ when $3\ \text{V} \geq x_m = z_n \geq 1.2\ \text{V}$ and $\alpha \leq 0$ when $-3\ \text{V} \leq x_m = z_n \leq -1.2\ \text{V}$. When $z_n = 0$, and $3\ \text{V} \geq x_m \geq 1.2$ V, or $-3\ \text{V} \leq x_m \leq -1.2$ V, the circuit executed the learning function $\dot{w}_{nm} = z_n\, x_m = 0$, and the inference function $I_{nm} = w_{nm}\, x_m$ concurrently. The operational voltages of synstors fall within the

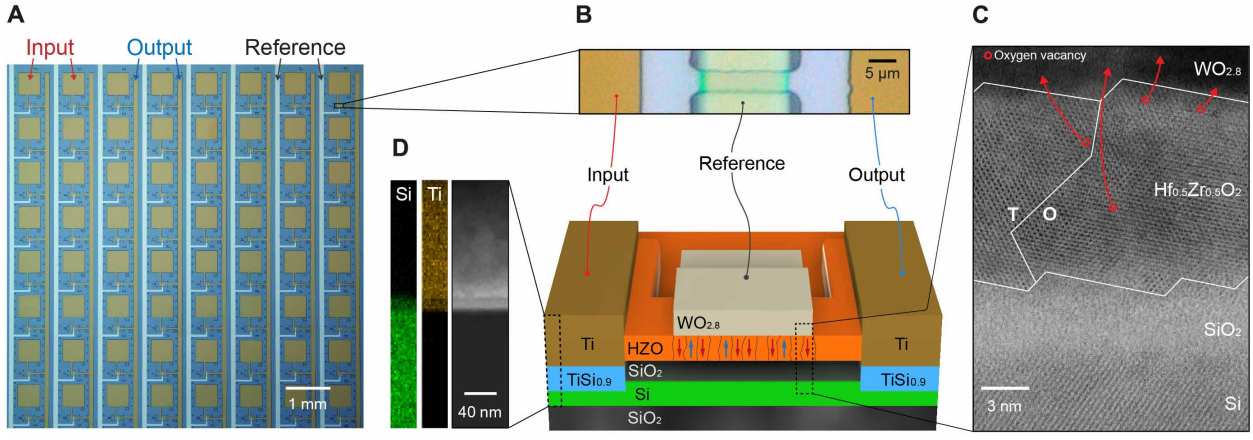

Fig. 2. Structure of a synstor circuit. (**A**) A top-view optical image shows an 8 × 8 synstor crossbar composed of eight rows of Ti input electrodes, eight columns of Ti output electrodes, and eight columns of $WO_{2.8}$ reference electrodes. (**B**) Top-view optical image (top) and a three-dimensional (3D) schematic illustration (bottom) of a synstor composed of a Si channel surrounded by SiO_2 layers, a $WO_{2.8}$ reference electrode grown on a $Hf_{0.5}Zr_{0.5}O_2$ layer on the SiO_2 layer on the Si channel. The Si channel is connected with a $TiSi_{0.9}$ layer and Ti input and output electrodes. The $Hf_{0.5}Zr_{0.5}O_2$ layer is composed of multiple ferroelectric domains, indicated by red or blue arrows, and dielectric domains, depicted without arrows. (**C**) Cross-sectional STEM image across the $WO_{2.8}/Hf_{0.5}Zr_{0.5}O_2/SiO_2/Si$ heterojunction with tetragonal (T) and orthorhombic (O) ferroelectric phases in the $Hf_{0.5}Zr_{0.5}O_2$ layer. The arrows illustrate the migrations of oxygen vacancies, represented as red open circles, from the $Hf_{0.5}Zr_{0.5}O_2$ layer to the $WO_{2.8}$ layer. (**D**) A cross-sectional STEM image (right) and EDX chemical maps of Ti and Si elements (left) across the $Ti/TiSi_{0.9}/Si$ heterojunction are displayed.

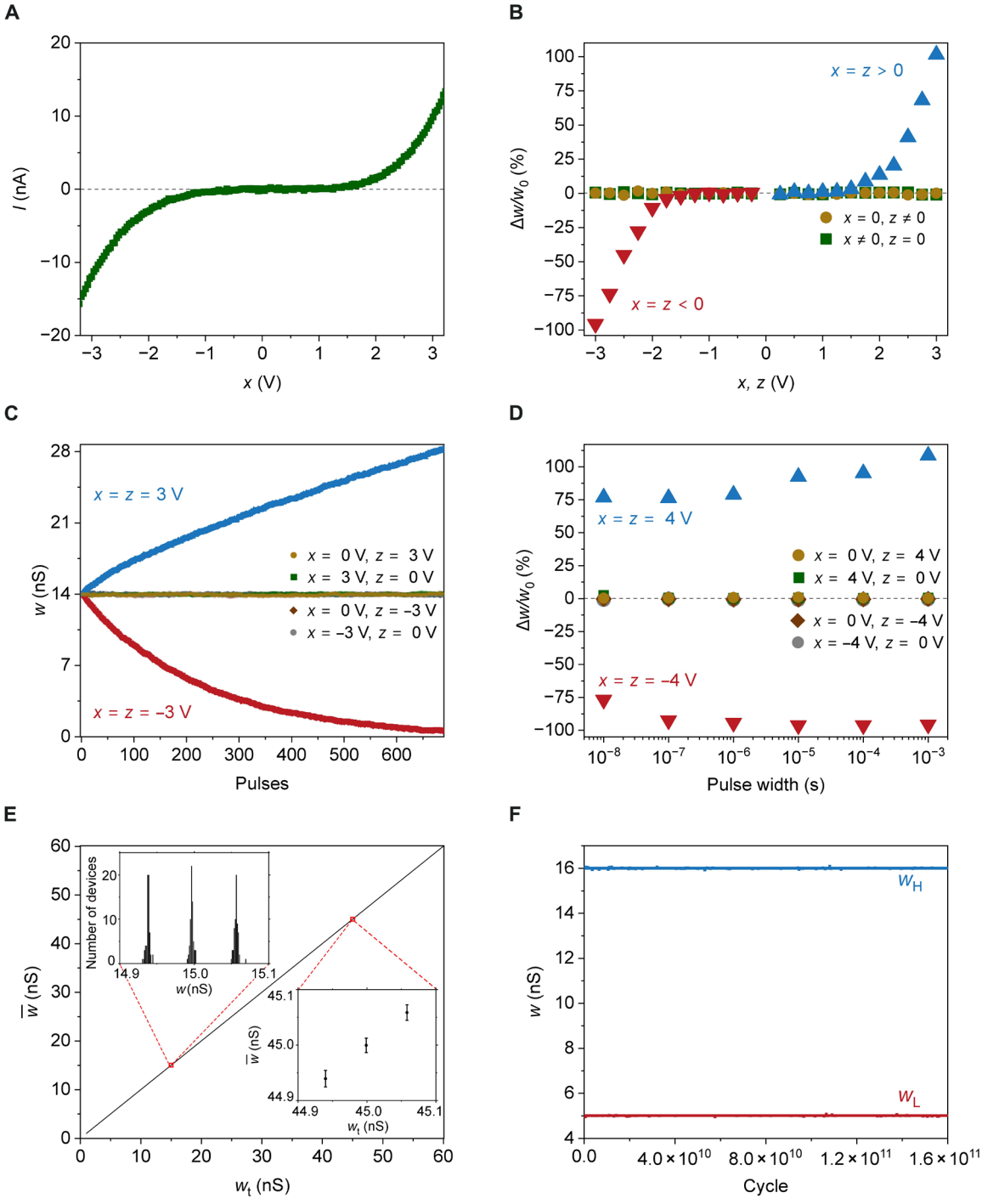

Fig. 3. Electric properties of synstors. (**A**) The current, I, on the output electrode of a synstor is displayed versus voltage, x, applied on the input electrode of the synstor with respect to its grounded output and reference electrodes. (**B**) The percentage changes in the synstor conductance, $(\Delta w/w_0) \times 100\%$, are plotted versus various x and z pulses concurrently applied on the input and output electrodes. (**C**) The changes in the synstor conductance, w, induced by various x and z pulses are plotted against the numbers of applied pulses. (**D**) The percentage changes in conductance w, $(\Delta w/w_0) \times 100\%$, of a synstor are shown against the widths of the applied x and z pulses on its input and output electrodes, respectively, after the synstor experienced pulses with a total duration of 500 ms and amplitudes $x = z = -4$ V (red triangles), $x = z = 4$ V (blue triangles), $x = 0$ and $z = 4$ V (brown circles), $x = 4$ V and $z = 0$ (green squares), $x = -4$ V and $z = 0$ (gray circles), and $x = 0$ and $z = -4$ V (brown diamonds). (**E**) The average analog conductance values, $\overline{w}$, of 64 synstors are plotted against 1000 targeted analog conductance values, w_t, evenly separated by $\Delta w_t = 59$ pS. The inset in the top-left corner shows the distribution of the synstor conductance values when $w_t = 14.938$, 14.997, and 15.056 nS. The inset in the bottom-right corner shows $\overline{w}$ with $\pm 3\sigma_w$ SDs against w_t at 44.940, 44.999, and 45.058 nS. (**F**) A synstor was iteratively modified to its high ($w_H = 16$ nS) and low ($w_L = 5$ nS) conductance values, which are displayed as blue and red squares, respectively, against the modification cycles.

operational voltage range (±3.8 V) of 22-nm CMOS (complementary metal-oxide semiconductor) circuits with HfZrO-based ferroelectric transistors (*40*).

The synstor conductance was also effectively modified by applying paired pulses with amplitudes $x = z = \pm 4$ V and widths ranging from 10 ns to 1 ms (Fig. 3D), indicating that the device conductance can be modified within 10 ns, which has also been observed in HfZrO-based transistors (*40*). The analog learning accuracy was assessed through the fine-tuning of 64 synstors in the circuit precisely toward 1000 distinct values, w_t, ranged between 1 and 60 nS and separated evenly by $\Delta w_t = 59$ pS by applying a train of paired $x_m = z_n$ pulses (Materials and Methods). As shown in Fig. 3E and fig. S3 (A and B), the disparities between the average conductance values of the 64 synstors and their respective w_t, $|\overline{w} - w_t|$, are smaller than 1.5 pS or 2.5% of Δw_t, and the SDs σ_w at different $\overline{w}$ are below 6 pS or 10% of Δw_t. As shown in fig. S3C, the 64 as-fabricated devices initially exhibited considerable variation in conductance, with an average conductance of 2.7 nS and an SD of 2.1 nS, but this variation was substantially reduced to an average of 1.531 nS and an SD of 0.001 nS after tuning the devices to a target conductance value ($w_t = 1.5315$ nS). The uniformity of conductance values w for the 64 synstors, tuned to the targeted conductance value ($w_t = 1.5315$ nS, $\overline{w} = 1.531$ nS, and $\sigma_w = 0.001$ nS), is significantly better than that of carbon nanotube (CNT)–based ($\overline{w} = 1.90$ nS and $\sigma_w = 0.45$ nS) (*35*) and Al oxide-based ($\overline{w} = 2.219$ nS and $\sigma_w = 0.062$ nS) (*37*) synstors (fig. S3D). The 1000 dynamically tunable conductance levels and the precise conductance modification accuracy of 36 pS ($6\sigma_w$) could be attributed to the progressive switching of the multiple individual nanoscale ferroelectric domains in the $Hf_{0.5}Zr_{0.5}O_2$ layer (Fig. 2C) (*39*, *41*). To assess their learning endurance, synstors were iteratively adjusted to their high ($w_t = 16$ nS) and low ($w_t = 5$ nS) conductance values (Materials and Methods). No degradation in device conductance was observed over 1.6×10^{11} switching cycles (Fig. 3F). Synstors were iteratively tuned to their maximum (60 nS) and minimum (0.6 nS) conductance values. No degradation in device conductance was observed over 1.1×10^9 switching cycles (fig. S3E). The distributions of the conductance values across the different tuning cycles are shown in fig. S3F, with $\overline{w} = 59.9998$ nS and $\sigma_w = 0.0907$ nS for the maximum conductance ($w_t = 60$ nS) and $\overline{w} = 0.6314$ nS and $\sigma_w = 0.0628$ nS for the minimum conductance ($w_t = 0.6$ nS). HZO-based devices typically degraded after ~10^6 switching cycles, mainly induced by oxygen vacancies in the $Hf_{0.5}Zr_{0.5}O_2$ layer (*39*, *40*). In the $WO_{2.8}$/$Hf_{0.5}Zr_{0.5}O_2$ heterojunction of the synstor, the oxygen vacancies with higher defect energy levels in the $Hf_{0.5}Zr_{0.5}O_2$ layer tended to migrate toward the W oxide layer with lower defect energy levels (Fig. 2C) (*44*), significantly enhancing the switching cycles of the $Hf_{0.5}Zr_{0.5}O_2$ layer and converting the W oxide layer to metallic reference electrode (*45*). The current (I) through the synstor was measured as a function of input voltage (x) over a temperature range of 24° to 80°C (Materials and Methods). No significant hysteresis was observed in the $I - x$ curves, indicating that the input voltage alone does not change the device conductance (fig. S3G). The conductance increases with increasing temperature due to the higher carrier concentration in the Si semiconducting channel. However, the conductance can be adjusted to maintain a constant target value across 24° to 80°C by applying paired x and z pulses, compensating for temperature-induced changes in carrier concentration (fig. S3H). The current-voltage characteristics and resistance of a $WO_{2.8}$ resistor were measured across a temperature range of 80 to 320 K (Materials and Methods). No notable change in resistance with temperature was observed in the Arrhenius plot (fig. S4A), and the linear current-voltage curves (fig. S4B) suggests the metallic conduction mechanism in $WO_{2.8}$ film. The resistivity of the $WO_{2.8}$ layer is estimated to be 5.0×10^{-6} ohms · m, which is comparable with previously reported values for defected tungsten oxide (*45*) and metals with high resistivity. The conductance values of synstors were measured at 40° and 85°C versus time after the synstors were modified by paired pulses (Materials and Methods and fig. S5, A and B). Similar to the dynamic changes of synaptic weights in neurobiological networks (*28*, *30*), the conductance values of the synstors changed at the initial testing stage, possibly due to incomplete charge compensation in the $Hf_{0.5}Zr_{0.5}O_2$ layer. However, the ferroelectric dipoles and device conductance values remained stable for long-term memory (*46*). The devices tested at 40°C exhibit distinguishable conductance states, whereas those tested at 85°C do not. The higher temperature likely induces significant fluctuations in the electric dipoles within the $Hf_{0.5}Zr_{0.5}O_2$ layer, leading to more random variations in conductance across different devices. However, dynamic adjustment of the device conductance and learning can compensate for and correct these temperature-induced conductance variations, as illustrated in fig. S3H.

The polarization (P) of a 10-nm-thick $Hf_{0.5}Zr_{0.5}O_2$ film was measured as a function of the applied voltage (V) across the film (Materials and Methods). The resulting P-V curve (fig. S6) demonstrates the ferroelectric properties of the $Hf_{0.5}Zr_{0.5}O_2$ film. The ability of the device to dynamically adjust its conductance in analog mode is attributed to the gradual switching of multiple nanoscale ferroelectric domains within the ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ layer (*39*, *41*). As shown in the simulated band structures of the synstor (Fig. 4), when a pair of positive or negative voltage pulses with magnitudes of $x = z = 3.0$ or −3.0 V are applied, an electric field is generated within the $Hf_{0.5}Zr_{0.5}O_2$ layer, reaching approximately $\mathbf{E} \approx 790$ or −790 kV / cm (Fig. 4, A and B). This electric field exceeds the critical positive and negative threshold values, $\mathbf{E} > \mathbf{E}_t^+$ or $\mathbf{E} < \mathbf{E}_t^-$, required to switch individual nanoscale ferroelectric domains in the $Hf_{0.5}Zr_{0.5}O_2$ layer. Under these conditions, the paired voltage pulses progressively switch the individual ferroelectric domains, altering their ferroelectric dipoles (with $\Delta\mathbf{P} > 0$ or $\Delta\mathbf{P} < 0$), and subsequently either attract or repel holes in the p-type Si channel. This adjustment in the ferroelectric dipoles results in an increase or decrease in the synstor conductance in analog mode (Fig. 3C). In contrast, when the synstor is subjected to a single voltage pulse with $x = 3$ V and $z = 0$, or $x = -3$ V and $z = 0$, or in the absence of pulses ($x = z = 0$), the electric potential primarily drops across the Schottky junction formed between the Si channel and the $TiSi_{0.9}$ layer (*43*). In this scenario, the electric field within the $Hf_{0.5}Zr_{0.5}O_2$ layer, which is located beyond the Schottky junction, becomes $\mathbf{E} = -4$, −153, or −3 kV / cm, respectively (Fig. 4D). Under these conditions, the electric field does not exceed the threshold values ($\mathbf{E}_t^- < \mathbf{E} < \mathbf{E}_t^+$), so it cannot modify the ferroelectric dipoles ($\Delta\mathbf{P} \approx 0$), and thus, the synstor conductance remains unchanged (Fig. 3, B and C).

Drone navigated by a synstor circuit and human operators

A synstor circuit navigated a drone toward a target position by avoiding obstacles in a simulated environment with time-varying strong wind (Materials and Methods, Fig. 5, fig. S7A, and

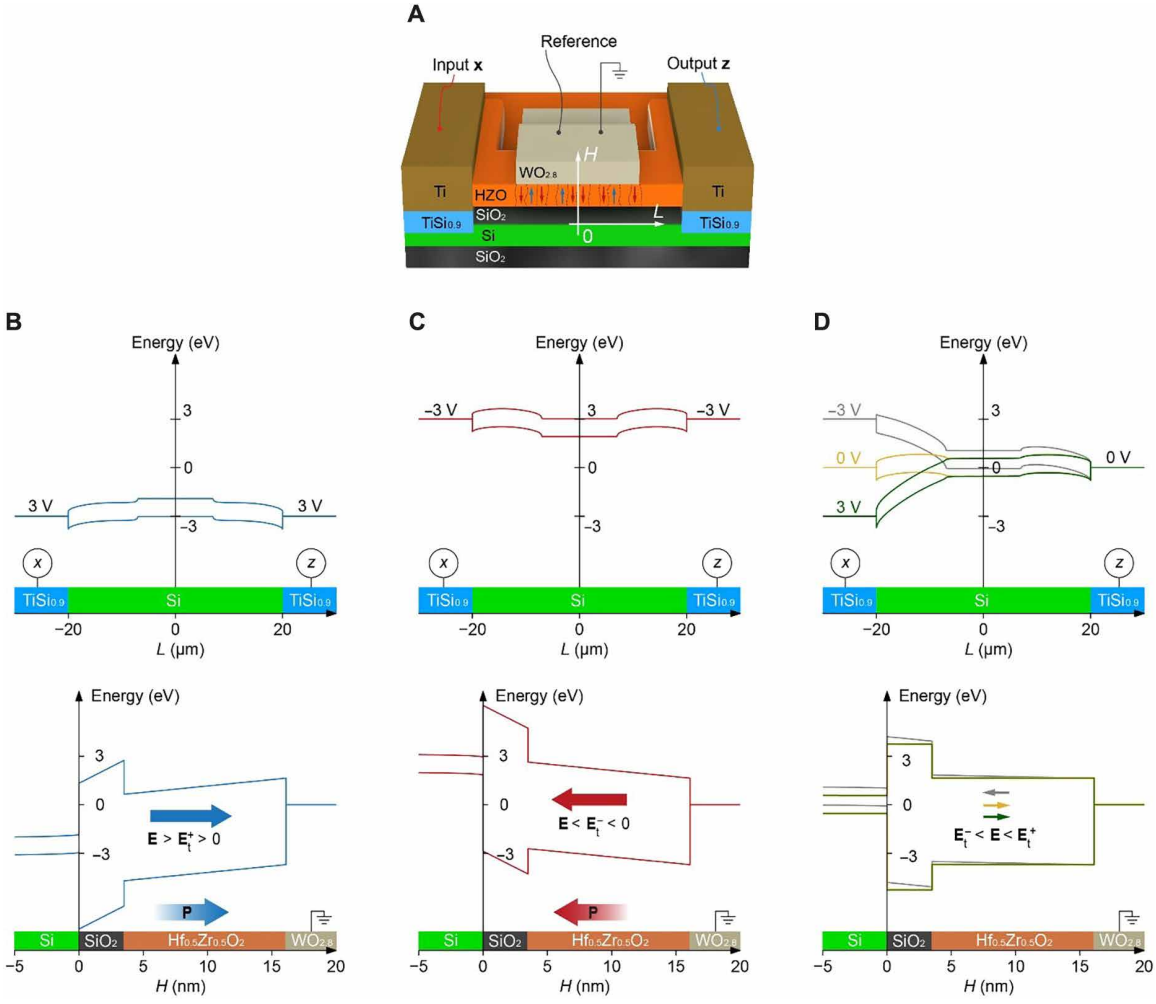

Fig. 4. Energy-band structures of a synstor. (**A**) 3D schematic illustration of a synstor composed of a grounded $WO_{2.8}$ reference electrode, $Hf_{0.5}Zr_{0.5}O_2$ layer, SiO_2 dielectric layer, and Si channel along the *H* axis and a $TiSi_{0.9}$ input electrode, Si channel, and $TiSi_{0.9}$ output electrode along the *L* axis. The $Hf_{0.5}Zr_{0.5}O_2$ layer is composed of multiple ferroelectric domains, indicated by red or blue arrows, and dielectric domains, depicted without arrows. The simulated energy-band structures along the *L* axis (top) and along the *H* axis (bottom) of a synstor under the conditions of (**B**) the potentials at the input electrode $x = 3$ V and the output electrode $z = 3$ V, (**C**) $x = z = -3$ V, and (**D**) $x = 3$ V and $z = 0$ (green lines), $x = -3$ V and $z = 0$ (gray lines), and $x = z = 0$ (yellow lines). The top scale (*L*) represents the lateral distance from the input electrode to the output electrode, and the bottom scale (*H*) represents the vertical distance from the Si channel to the W reference electrode (also shown in Fig. 1D). When the electric field, **E**, in the $Hf_{0.5}Zr_{0.5}O_2$ layer satisfies $\mathbf{E} > \mathbf{E}_t^+ > 0$ in (B), or $\mathbf{E} < \mathbf{E}_t^- < 0$ in (C), with $\mathbf{E}_t^+$ and $\mathbf{E}_t^-$ as the positive and negative electric threshold fields to switch the polarization of the individual ferroelectric domains in the $Hf_{0.5}Zr_{0.5}O_2$ layer, leading to the changes of the dipole density, $\Delta\mathbf{P} > 0$ or $\Delta\mathbf{P} < 0$. When $\mathbf{E}_t^- < \mathbf{E} < \mathbf{E}_t^+$ in (D), $\Delta\mathbf{P} \approx 0$.

movie S1). Obstacles were detected by a simulated camera on the drone, and a moving target position ($\hat{\mathbf{s}}$) was identified to avoid the obstacles and minimize an objective function $F = \frac{1}{2}(\mathbf{s} - \hat{\mathbf{s}})^2$, with $\mathbf{s} - \hat{\mathbf{s}}$ as the deviations of the drone position ($\mathbf{s}$) from its target positions (Materials and Methods and fig. S7D). In the windy environment, the speeds and directions of winds changed randomly during the flight (fig. S8A). During the synstor experiments, $\mathbf{s} - \hat{\mathbf{s}}$ was converted to input voltage pulses, $\mathbf{x}$, by an interface circuit to generate currents via the synstor circuit according to its inference function, $\mathbf{I} = \mathbf{W}\mathbf{x}$ (Eq. 1). The currents triggered actuation signals, $\mathbf{y}$, via a neuron and an interface circuit to drive the drone. The conductance matrixes ($\mathbf{W}$) of the synstor circuit were initialized to random values before each experiments started (Materials and Methods and fig. S10) to ensure that the circuit had no prior learning experience or predefined function. Concurrently, voltage pulses, $\mathbf{z}$, meeting the conditions $\overline{\mathbf{z}} = 0$ (Materials and Methods and Eq. 3) and $\overline{z_n y_n} \leq 0$ (Materials and Methods and Eq. 4) were triggered at the output electrodes of the synstor circuit (Materials and Methods) to modify $\mathbf{W}$ according to the learning rule $\dot{\mathbf{W}} = \alpha\, \mathbf{z} \otimes \mathbf{x}$ (Eq. 2) during the real-time learning process in a Super-Turing computing mode.

Human operators also navigated a drone toward the target position by avoiding obstacles in the same simulated windy environment (Materials and Methods, Fig. 5, figs. S7B and S8B, and movie S1). The human operators had no prior experience with the drone control system, ensuring that they learned while navigating the drone. During the human experiments, the operators visually saw the analog numbers $\mathbf{s} - \hat{\mathbf{s}}$ displayed on a monitor and manually triggered an actuation signal $\mathbf{y}$ from a keyboard to drive the drone. Concurrently, the synaptic weight matrixes $\mathbf{W}$ could be modified using the synaptic learning function (*26*, *28*, *30*) $\dot{\mathbf{W}} = \alpha\, \mathbf{z} \otimes \mathbf{x}$ during the real-time learning process.

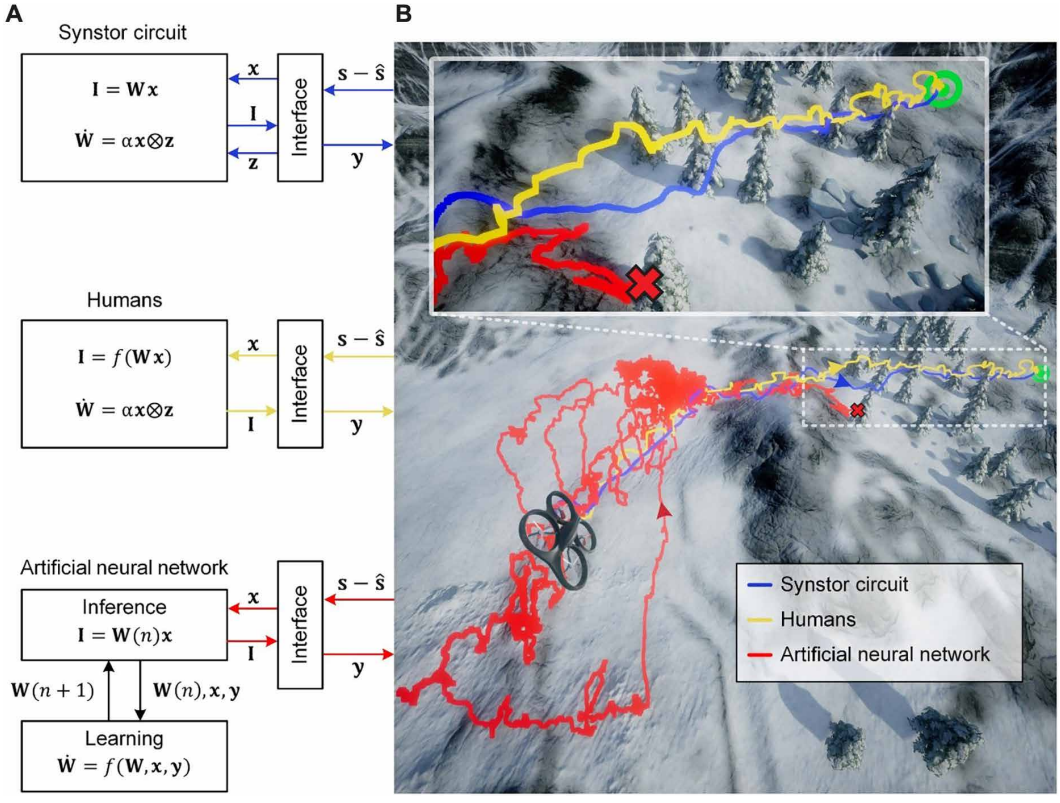

Fig. 5. Experiments to negative a drone by a synstor circuit, human operators, and an ANN. (**A**) A synstor circuit (top), humans (middle), and a computer-based ANN (bottom) (**B**) drive a drone toward a target position by avoiding obstacles in a simulated windy environment. The starting point of the flights is marked by a drone image, and the final target position is marked by a green target symbol. The flying traces are shown for the drone driven by the synstor circuit (blue line), the human (yellow line), and the ANN (red line). The inset shows the details in the area near the target with tree obstacles. The red crash symbols indicate that the drone crashed into trees.

Drone navigated by a computer-based ANN

In the control experiments for computer-based ANN to navigate a drone toward the target position by avoiding obstacles in the simulated windy environment, various ANN structures and learning parameters were tested, and the optimal ANN with the shortest learning time was then deployed to navigate the drone (Materials and Methods, Fig. 5, figs. S7C, S8C, and S10, and movie S1). The time required to execute the learning algorithm was significantly longer than that to execute the inference algorithm (fig. S10F); thus, it was infeasible to execute real-time learning on the computer, and the inference and learning had to be executed sequentially. The $\mathbf{s}-\hat{\mathbf{s}}$ signals were converted to input signals, $\mathbf{x}$, and induced output currents $\mathbf{I}=\mathbf{W}(n)\,\mathbf{x}$, triggering actuation signals, $\mathbf{y}$, from the ANN to drive the drone in its nth flight episode. The saved experimental data $\mathbf{x}$, $\mathbf{y}$, and $\mathbf{W}(n)$ from the nth episode were sent back to the computer to execute a reinforcement learning algorithm (*47*) (Materials and Methods) to modify $\mathbf{W}(n)$ to $\mathbf{W}(n+1)$, which reset the ANN to drive the drone at the $(n+1)$th flight episode iteratively until the drone crashed into an obstacle or reached the final target (Fig. 5 and fig. S7C).

Learning time, performance, adaptability, and power consumption

The synstor circuit, human operators, and ANN successfully learned to drive the drone toward its target position across the mountain area without trees or strong wing while minimizing the objective function $F=\frac{1}{2}\left(\mathbf{s}-\hat{\mathbf{s}}\right)^2$. The $F-t$ curves can be best fitted by $F(t)=\left[F(0)-F_e\right]e^{-t/T_L}+F_e$ (Materials and Methods, Eq. 6, and Fig. 6) to extrapolate the average learning time T_L and the equilibrium objective function F_e when $t\gg T_L$ and $d\overline{F}/dt\approx 0$, which represents the performance of the drone when $\mathbf{W}$ has been modified to $\widehat{\mathbf{W}}$. The average T_L (4.4 s) of the synstor circuit in multiple trials was shorter than the average T_L (6.6 s) of the human operators and significantly superior to the average T_L (127,568 s) of the ANN in multiple trials (Fig. 6D). The drone performance, represented by F_e, of the drone driven by the synstor circuit [0.10 arbitrary unit (a.u.)] and humans (0.25 a.u.) is significantly superior to that of the drone driven by the ANN (0.44 a.u.) in their multiple trials (Fig. 6E). When the drone entered the environment with trees and strong wind, only the synstor circuit and most human operators were able to navigate the drone to its final target position, demonstrating their ability to adapt to the environment with the gale and avoid collisions with the trees; in contrast, the ANN consistently failed to adapt to the complex environment with trees and gale, resulting in collisions in multiple trials (Fig. 6, A to C, and movie S1). The adaptability to the changing environment is evaluated by the success rate of learning to drive the drone to its final target without collisions in multiple trials. The adaptability (100%) of the synstor circuit is better than that (64%) of the human operators and significantly superior to that (0%) of the ANN (Fig. 6F). The power consumption of the synstor circuit (158 nW; Materials and Methods) for the concurrent execution of the inference and learning algorithms was also seven orders of magnitude lower than the aggregate power consumption of the computer

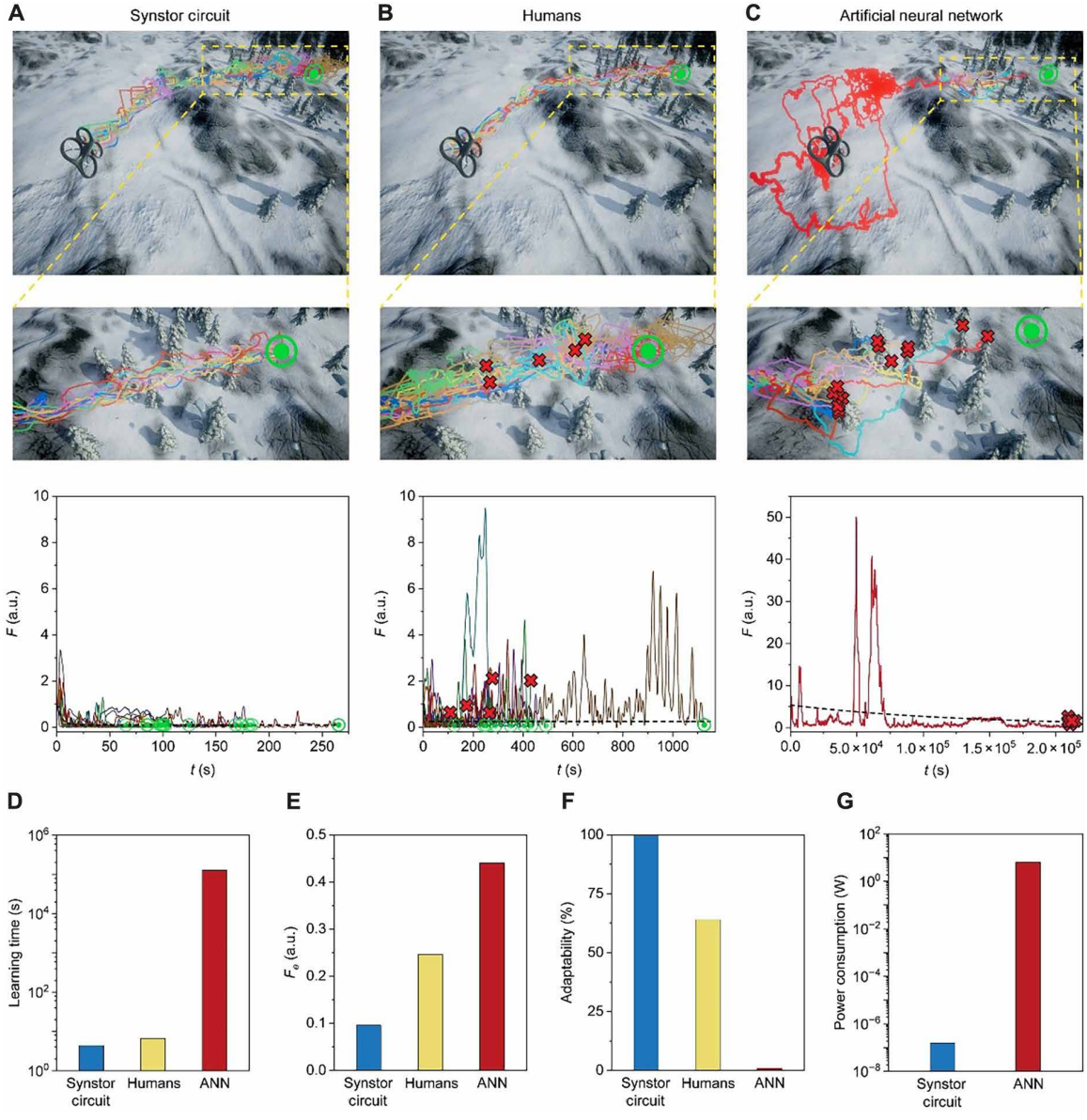

Fig. 6. Experimental results of drone navigations. (Top row) The flying traces are shown for a drone driven by (**A**) a synstor circuit, (**B**) human operators, and (**C**) an ANN toward a target position by avoiding obstacles in a simulated windy environment. The starting point of the flights is marked by drone images. (Middle row) The zoom-in images show the details of the flying traces in the area near the target with tree obstacles. (Bottom row) Objective functions, $F = \frac{1}{2}(\mathbf{s}-\hat{\mathbf{s}})^2$, with $\mathbf{s}-\hat{\mathbf{s}}$ as the deviations of the drone position ($\mathbf{s}$) from its target position ($\hat{\mathbf{s}}$) versus accumulative flight and learning time t. The $F-t$ curves are best fitted by $F(t) = [F(0)-F_e]\ e^{-t/T_L} + F_e$ (dashed lines). The red crash symbols indicate that the drone crashed into the tree, and the final target position is marked by green target symbols. Comparison of average (**D**) learning time (T_L), (**E**) equilibrium objective function (F_e), (**F**) adaptability to the changing environment, and (**G**) computing power consumption of the synstor circuit, human operators, and ANN in multiple trials. The adaptability to changing environment is evaluated by the successful rate of learning how to drive the drone to its final target without collisions in multiple trials. The power consumption of the synstor circuit is for concurrent inference and learning, whereas the power consumption of the ANN is the aggregate of the power consumptions for sequential inference and learning.

(6.3 W; Materials and Methods) executing the learning and inference algorithms sequentially (Fig. 6G). Estimating the power consumption of the human brain for the inference and learning is difficult.

DISCUSSION

We introduced an intelligent system based on a synstor circuit with concurrent real-time inference ($\mathbf{I} = \mathbf{W}\mathbf{x}$; Eq. 1) and learning ($\dot{\mathbf{W}} = \alpha\, \mathbf{z} \otimes \mathbf{x}$; Eq. 2) functionality emulating the brain. Theoretical analysis indicates that the simultaneous execution of inference and learning can minimize the objective function $F = \frac{1}{2}(\mathbf{s}-\hat{\mathbf{s}})^2$ of the system, tuning the system states ($\mathbf{s}$) toward their target states ($\hat{\mathbf{s}}$) by modifying $\mathbf{W}$ toward $\widehat{\mathbf{W}} = arg\ \min_{\mathbf{W}} F$. A circuit of three-terminal synstors was fabricated by integrating a heterojunction of a Si channel/SiO_2 dielectric layer/defect-reduced ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ layer/defect-enhanced $WO_{2.8}$ reference electrode vertically, and Schottky contacts between the Si channel/$TiSi_{0.9}$/Ti input and output

electrodes laterally in each synstor. Paired voltage pulses (x_m and z_n) applied on the input and output electrodes of a synstor with respect to a grounded reference electrode progressively modify the individual ferroelectric domains within the $Hf_{0.5}Zr_{0.5}O_2$ layer, thereby adjusting the synstor conductance in analog mode based on the learning function ($\dot{\mathbf{W}} = \alpha\, \mathbf{z} \otimes \mathbf{x}$); a single voltage pulse (x_m) applied to the input electrode of a synstor induces a current through the synstor channel according to the inference function ($\mathbf{I} = \mathbf{W}\mathbf{x}$). The voltage primarily drops laterally across the Schottky junction and does not modify the ferroelectric domains within the $Hf_{0.5}Zr_{0.5}O_2$ layer or the synstor conductance (i.e., $\dot{w}_{nm} = 0$ when $x_m \neq 0$ and $z_n = 0$) as per the learning rule ($\dot{\mathbf{W}} = \alpha\, \mathbf{z} \otimes \mathbf{x}$). Compared to other neuromorphic devices like two-terminal memristors and ferroelectric devices, which can only perform inference and learning sequentially, the synstor circuit uniquely enables concurrent execution of inference and learning, allowing the circuit to operate in a Super-Turing mode (Table 1). The defect-reduced $Hf_{0.5}Zr_{0.5}O_2$ layer with multiple switchable ferroelectric domains effectively improves the device performance and facilitates the precise, reliable, fast, and repetitive modification of synstor conductance with 1000 analog conductance levels within a conductance range of 0 to 60 nS, a learning accuracy of 36 pS, 1.6×10^{11} repetitive learning cycles, and a rapid modification time within 10 ns. In experiments aimed at navigating a drone toward target positions while avoiding obstacles in a simulated complex aerodynamic environment with time-varying wind, without any prior learning, a synstor circuit and human operators executed real-time learning and inference concurrently, in comparison with an ANN run on a computer executing inference and learning sequentially in Turing mode. During concurrent real-time inference and learning in a synstor circuit, the conductance (w_{nm}) of each synstor can be dynamically adjusted based on signals (x_m and z_n) received from the input and output electrodes connected by the synstor in parallel analog mode. The learning process aims to optimize the objective function (F) in response to environmental changes in real time. In contrast, during sequential inference and learning processes in the ANN or other neuromorphic resistor circuits, their weight matrixes cannot be adjusted during inference according to real-time environmental changes. The optimal weight matrices were derived during iterative learning processes with serial statistical evaluation and modification of numerous various combinations of **W** elements. The experimental learning times (T_L) for both the synstor circuit and human operators was four orders of magnitude shorter than those of the ANN. The ANN consistently was unable to adapt to the complex environment with trees and strong variable winds, resulting in collisions in every trials. In contrast, the synstor circuit and most human operators successfully adapted to the environment, driving the drone to its final target without collisions. As evaluated by the equilibrium objective function (F_e) when **W** has been modified to $\widehat{\mathbf{W}}$, the performance of the drone driven by the synstor circuit and human operators was significantly superior to that of the drone driven by the ANN. A single-layer synstor circuit can execute learning and inference concurrently in real time, dynamically optimizing the **W** matrix, triggering optimal output actuation signals (**y**) to minimize the objective function (F). Conversely, during the sequential inference and learning processes, the ANN expended large amounts of energy and time to store the weight matrix, **x**, and **y** data, execute the learning functions in its computing units, and transfer the data back and forth between different circuits (*4*–*7*, *12*, *13*, *15*, *17*–*19*, *22*). The conductance of the synstors (< 60 nS) was significantly lower than that of transistors (~0.1 mS) (*5*–*7*, *48*), memristors (~1 μS to 10 mS) (*15*, *17*, *49*–*52*), and phase change memory resistors (1 μS to 10 mS) (*22*) (fig. S11). Consequently, the power consumption of synstors is significantly lower than that of other neuromorphic devices (Table 1). The power consumption of the synstor and neuron circuits (158 nW) for real-time concurrent inference and learning was seven orders of magnitude lower than the aggregate power consumption (6.3 W) of the computer executing the learning and inference functions sequentially in the ANN. The computing energy efficiency of the synstor circuit is calculated (Materials and Methods) as 1.2×10^{17} operations per second per watt (OPS/W), which is significantly higher than those of other

Table 1. Comparison of devices. Comparative analysis of synstors (this work) alongside biological synapses (*28*), ferroelectric transistors (*38*, *40*, *41*, *53*), and memristors (*17*, *18*, *49*, *51*).

	Synstor (this work)	Synapse	Ferroelectric transistor	Memristor
Learning and inference signal magnitudes	Same	Same	Different	Different
Concurrent learning and inference	Yes	Yes	No	No
Turing mode	Yes	Yes	Yes	Yes
Super-Turing mode	Yes	Yes	No	No
Real-time adaptability	Yes	Yes	No	No
Real-time error correction	Yes	Yes	No	No
Conductance (S)	$<6 \times 10^{-8}$	$\sim 10^{-11}$–10^{-9}	$<10^{-5}$	$<10^{-4}$
Power consumption (W)	2.5×10^{-9}	$\sim 10^{-13}$–10^{-11}	$\sim 10^{-6}$	$\sim 4 \times 10^{-6}$
Energy efficiency (OPS/W)	1.2×10^{17}	$\sim 10^{15}$–10^{17}	5.7×10^{13}	1.9×10^{14}
Device area (mm^2)	2×10^{-4}		3.6×10^{-8}	2.5×10^{-7}
Area efficiency (OPS/mm^2)	1.5×10^{12}		1.6×10^{15}	7.2×10^{12}
Endurance (switching cycles)	$>10^{11}$		$>10^{8}$	$>10^{12}$

neuromorphic devices. However, the area of the microscale synstor (2×10^{-4} mm^2) is considerably larger than those of nanoscale neuromorphic devices, leading to a much lower area efficiency (1.5×10^{12} OPS/mm^2; Materials and Methods) compared with nanoscale neuromorphic devices (Table 1). Scaling down the synstors could further reduce their conductance, power consumption, and area, thereby enhancing both energy and area efficiency. On the basis of simulations (Materials and Methods), a HfZrO-based synstor can be scaled down to a channel length of 100 nm (fig. S12), and a HfZrO-based synstor crossbar circuit can be scaled up to 10^8 synstors with 10^4 input and output channels using the nanoscale fabrication techniques of the HfZrO-based ferroelectric transistor circuit (*40*, *53*). Synstor circuits offer a brain-inspired Super-Turing computing platform for AI systems with extremely low power consumption, high-speed real-time learning and inference, and agile adaptability to dynamic complex environments.

MATERIALS AND METHODS

Theoretical analysis of a synstor circuit

The temporal mean of the $\mathbf{z}$ voltage pulses applied on the output electrode of the synstor circuit satisfies

$$\overline{\mathbf{z}} = 0 \tag{3}$$

and the covariance between z_n and $y_{n'}$

$$\overline{z_n y_{n'}} = \eta_n \, \delta_{nn'} \tag{4}$$

where $\delta_{nn'}$ denotes the Kronecker delta with $\delta_{nn'} = \begin{cases} 0 \text{ when } n' \neq n \\ 1 \text{ when } n' = n \end{cases}$, and η_n denotes a parameter. The covariance $\overline{z_n y_n}$ is defined as the mean of the product of the deviations of z_n and y_n from their individual means $\overline{z}_n$ and $\overline{y}_n$. $\overline{z_n y_{n'}} = \overline{(z_n - \overline{z}_n)(y_{n'} - \overline{y}_{n'})} = \overline{z_n (y_{n'} - \overline{y}_{n'})}$, where $\overline{z}_n = 0$ (Eq. 3) and $\overline{z_n \overline{y}_{n'}} = \overline{z}_n \overline{y}_{n'} = 0$. The learning rule observed in synapses within neurobiological circuits, known as STDP (*28*, *30*), can also be formulated as $\frac{d\mathbf{W}}{dt} = \alpha \, \mathbf{z}(t) \otimes \mathbf{x}(t)$ (Eq. 2) with $z_n(t) = \begin{cases} A_- e^{(t - t_n^y)/\tau_-} \text{ when } t < t_n^y \\ -A_+ e^{-(t - t_n^y)/\tau_+} \text{ when } t \geq t_n^y \end{cases}$, where t_n^y denotes the moment when a pulse ($\mathbf{y}$) is triggered at the nth postsynaptic neuron, $A_+ > 0$ and $A_- > 0$ denote amplitude constants, and $\tau_+ > 0$ and $\tau_- > 0$ denote time constants. In STDP, $\mathbf{z}$ fulfills the conditions $\overline{\mathbf{z}} = 0$ (Eq. 3) and $\overline{z_n y_{n'}} = \eta_n \, \delta_{nn'}$ (Eq. 4) with $\eta_n \geq 0$ for STDP and $\eta_n \leq 0$ for anti-STDP (*30*). The change rate of the output current (I_n) due to learning, $\left(\frac{\partial I_n}{\partial t}\right)_L = \sum_m \frac{\partial I_n}{\partial w_{nm}} \dot{w}_{nm} = \sum_m x_m (\alpha z_n x_m) = 2 |\alpha| \, z_n F_{\mathbf{x}}$, where $\frac{\partial I_n}{\partial w_{nm}} = x_m$ due to $I_n = \sum_m w_{nm} x_m$ (Eq. 1), $\dot{w}_{nm} = \alpha z_n x_m$ (Eq. 2), and $F_{\mathbf{x}} = \frac{1}{2} \sum_m x_m^2$. Although it is unfeasible to predefine a mathematical model for the correlation between $F_{\mathbf{x}}$ and y_n that is dynamically changing, a linear model can be constructed to describe their relationship during a learning period, $F_{\mathbf{x}} = \sum_n \left(\frac{\partial F_{\mathbf{x}}}{\partial y_n}\right)_L y_n + F_{\mathbf{x}}^0$. In the model, $\frac{\partial F_{\mathbf{x}}}{\partial y_n} = \left(\frac{\partial F_{\mathbf{x}}}{\partial y_n}\right)_L$ denotes the regression coefficient during the learning period, and $F_{\mathbf{x}}^0$ represents the portion of $F_{\mathbf{x}}$ that is not correlated with $\mathbf{y}$ or $\mathbf{z}$. On the basis of the linear model, $\overline{z_n F_{\mathbf{x}}} = \sum_{n'} \left(\frac{\partial F_{\mathbf{x}}}{\partial y_{n'}}\right)_L \overline{z_n y_{n'}} + \overline{z_n F_{\mathbf{x}}^0} = \left(\frac{\partial F_{\mathbf{x}}}{\partial y_n}\right)_L \overline{z_n y_n}$, where $\overline{z_n F_{\mathbf{x}}^0} = \overline{z}_n \overline{F_{\mathbf{x}}^0} = 0$, and $\overline{z_n y_{n'}} = 0$ for $n' \neq n$ (Eq. 4). The average change rate of I_n due to learning during the learning period $\overline{\left(\frac{\partial I_n}{\partial t}\right)_L} = 2 |\alpha| \, \overline{z_n F_{\mathbf{x}}} = 2 |\alpha| \left(\frac{\partial F_{\mathbf{x}}}{\partial y_n}\right)_L \overline{z_n y_n}$, where $\overline{z_n F_{\mathbf{x}}}$ is substituted by $\left(\frac{\partial F_{\mathbf{x}}}{\partial y_n}\right)_L \overline{z_n y_n}$. On the basis of the linear model, the average change rate of the objective function $F = \frac{1}{2}(\mathbf{s} - \widehat{\mathbf{s}})^2$ due to learning during the learning period $\overline{\left(\frac{\partial F}{\partial t}\right)_L} = \overline{\frac{\partial F}{\partial F_{\mathbf{x}}} \sum_n \frac{\partial F_{\mathbf{x}}}{\partial y_n} \frac{\partial y_n}{\partial I_n} \left(\frac{\partial I_n}{\partial t}\right)_L} = \left(\frac{\partial F}{\partial F_{\mathbf{x}}}\right)_L \left(\frac{\partial F_{\mathbf{x}}}{\partial y_n}\right)_L \left(\frac{\partial y_n}{\partial I_n}\right)_L \overline{\left(\frac{\partial I_n}{\partial t}\right)_L} = 2 |\alpha| \left(\frac{\partial F}{\partial F_{\mathbf{x}}}\right)_L \sum_n \left(\frac{\partial F_{\mathbf{x}}}{\partial y_n}\right)_L^2 \left(\frac{\partial y_n}{\partial I_n}\right)_L \overline{z_n y_n}$, where $\frac{\partial F}{\partial F_{\mathbf{x}}} = \left(\frac{\partial F}{\partial F_{\mathbf{x}}}\right)_L$ denotes the regression coefficient in the linear model $F = \left(\frac{\partial F}{\partial F_{\mathbf{x}}}\right)_L F_{\mathbf{x}} + F^0$ with F^0 as the portion of F that is not correlated with $F_{\mathbf{x}}$, $\frac{\partial y_n}{\partial I_n} = \left(\frac{\partial y_n}{\partial I_n}\right)_L$ denotes the regression coefficient in the linear model $y_n = \left(\frac{\partial y_n}{\partial I_n}\right)_L I_n + I_n^0$ with I_n^0 as the portion of I_n that is not correlated with y_n, and $\overline{\left(\frac{\partial I_n}{\partial t}\right)_L}$ is substituted by $2 |\alpha| \left(\frac{\partial F_{\mathbf{x}}}{\partial y_n}\right)_L \overline{z_n y_n}$. F is a monotonically increasing function of $F_{\mathbf{x}}$; thus, $\left(\frac{\partial F}{\partial F_{\mathbf{x}}}\right)_L \geq 0$. y_n is a monotonically increasing function of I_n; thus, $\left(\frac{\partial y_n}{\partial I_n}\right)_L \geq 0$. $\overline{\left(\frac{\partial F}{\partial t}\right)_L} = 2 |\alpha| \left(\frac{\partial F}{\partial F_{\mathbf{x}}}\right)_L \sum_n \left(\frac{\partial F_{\mathbf{x}}}{\partial y_n}\right)_L^2 \left(\frac{\partial y_n}{\partial I_n}\right)_L \overline{z_n y_n}$ with $2 |\alpha| \left(\frac{\partial F}{\partial F_{\mathbf{x}}}\right)_L \left(\frac{\partial F_{\mathbf{x}}}{\partial y_n}\right)_L^2 \left(\frac{\partial y_n}{\partial I_n}\right)_L \geq 0$ and $\overline{z_n y_n} \leq 0$ (Eq. 4); therefore, $\overline{\left(\frac{\partial F}{\partial t}\right)_L} \leq 0$. The average change rate of the objective function $\overline{\left(\frac{dF}{dt}\right)} = \overline{\left(\frac{\partial F}{\partial t}\right)_L} + \overline{\left(\frac{\partial F}{\partial t}\right)_0}$ with $\overline{\left(\frac{\partial F}{\partial t}\right)_0}$ as the average change rate of F not related to learning (i.e., without $\mathbf{W}$ modification). When $\mathbf{s} = \widehat{\mathbf{s}}$, $F = \frac{1}{2}(\mathbf{s} - \widehat{\mathbf{s}})^2 = 0$, $\mathbf{x} = 0$, $\dot{\mathbf{W}} = \alpha \, \mathbf{z} \otimes \mathbf{x} = 0$ (Eq. 2), and $\mathbf{W}$ reaches the optimal steady value $\widehat{\mathbf{W}} = arg \min_{\mathbf{W}} F$. When $\mathbf{W} \neq \widehat{\mathbf{W}}$, $\mathbf{s} \neq \widehat{\mathbf{s}}$; thus, $F = \frac{1}{2}(\mathbf{s} - \widehat{\mathbf{s}})^2 > 0$. When $\overline{\left(\frac{\partial F}{\partial t}\right)_L} \leq -\overline{\left(\frac{\partial F}{\partial t}\right)_0} \leq 0$

$$\overline{\left(\frac{dF}{dt}\right)} \leq 0 \tag{5}$$

$\overline{F}$ represents a Lyapunov function. When $\overline{\left(\frac{dF}{dt}\right)} < 0$, $\overline{F}$ is asymptotically decreased, thus resulting in modification of $\mathbf{W}$ toward $\widehat{\mathbf{W}} = arg \min_{\mathbf{W}} F$ during concurrent learning and inference processes.

The concurrent execution of the inference (Eq. 1) and learning (Eq. 2) in the synstor circuit tends to minimize the average objective function $\overline{F}$ over time. When the covariance between $\mathbf{z}$ and $\mathbf{x}$, $\overline{\mathbf{z} \otimes \mathbf{x}} = 0$, then $\overline{\frac{d\mathbf{W}}{dt}} = 0$, $\overline{\left(\frac{dF}{dt}\right)} = 0$, and $\mathbf{W} = \widehat{\mathbf{W}} = arg \min_{\mathbf{W}} F$ remain unchanged during the execution of the inference function, $\mathbf{I} = \widehat{\mathbf{W}} \mathbf{x}$.

Synstor circuit fabrication process

The fabrication process of a synstor circuit is depicted in fig. S1. The synstor circuit was fabricated on a silicon-on-insulator chip with a 220-nm-thick p-type Si layer with a boron doping concentration of 10^{15}/cm^3 on a 3-μm-thick buried silicon oxide layer on a 725-μm-thick Si wafer. A photoresist layer was patterned on the Si surface as an etching mask by ultraviolet (UV) photolithography. As shown in fig. S1A, a 5-μm-wide Si channel was made by reactive ion

etching (RIE; Oxford Plasmalab 80 Plus RIE). The photoresist was stripped with acetone, isopropanol, and deionized water. The wafer was cleaned using the standard Radio Corporation of America (RCA) cleaning process. As shown in fig. S1B, the surface of the Si channel was oxidized in a thermal oxidation furnace at 900°C in O_2 for 10 s to grow a 3.5-nm-thick SiO_2 layer. A photoresist layer was patterned by UV photolithography on the surface of the SiO_2 layer, and the photoresist patterns were used as an etching mask to etch the SiO_2 layer by RIE (Oxford Plasmalab 80 Plus RIE) in the contact areas for input/output electrodes (fig. S1C). A 300-nm-thick Ti layer was deposited by electron beam evaporation (CHA Industries Mark 40), and Ti input/output electrodes in the contact areas were made by lifting off a prepatterned photoresist layer (fig. S1D). A 40-nm-thick Al_2O_3 sacrificial layer was grown on the chip by atomic layer deposition (ALD; Fiji Ultratech ALD). The chip was annealed in forming gas (5% H_2 in N_2) at 460°C for 30 min to form a titanium silicide layer sandwiched between the Si channel and Ti input/output electrodes (fig. S1E). The Al_2O_3 sacrificial layer protected the materials from undesirable oxidation during the annealing. After the annealing, the sacrificial layer was selectively etched away with a 3% tetramethylammonium hydroxide aqueous solution. A 12.6-nm-thick $Hf_{0.5}Zr_{0.5}O_2$ layer was deposited on the chip by ALD (Fiji Ultratech ALD) at 200°C using tetrakis(dimethylamino) hafnium(IV) and tetrakis(dimethylamino)zirconium(IV) precursors (fig. S1F). An 80-nm-thick W oxide layer was deposited on the $Hf_{0.5}Zr_{0.5}O_2$ layer by magnetron sputtering (Denton Discovery), and W oxide reference electrodes were patterned by lifting off a photoresist layer (fig. S1G). The chip was then annealed in a rapid thermal annealing system (Modular Process Technology RTP-600xp) at 500°C for 1 min to crystalize and induce a heterojunction between ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ layer and a $WO_{2.8}$ reference electrode. Last, the $Hf_{0.5}Zr_{0.5}O_2$ layer on the contact pads of the input/output electrodes was etched away using photolithography and RIE (Oxford Plasmalab 80 Plus RIE).

Material characterization and electrical tests of synstors

Structural and material composition profiles of the synstor chip were characterized using STEM, EDX, and EELS analysis. EDX analysis was performed using JEOL JEM-2800 TEM operated at 200 kV. Atomic-resolution STEM and EELS analysis was performed with a JEOL Grand ARM TEM operated at 300 kV with a spherical aberration corrector. During the electric tests, the reference electrodes of the synstors and control devices were always grounded. Current-voltage characteristics were measured with a Keithley 4200 semiconductor parameter analyzer. The electrical voltage pulses applied to the input and output electrodes of the devices and circuits were generated by a field-programmable gate array (FPGA; National Instruments, cRIO-9063), computer-controlled modules (National Instruments, NI-9264), and a Tektronix AFG3152C waveform/function generator. Currents flowing through the synstors were measured by a semiconductor parameter analyzer, computer-controlled circuit modules (National Instruments, NI-9205 and NI-9403), and oscilloscope (Tektronix TDS 3054B). Testing protocols were programmed (NI LabVIEW) and implemented in an embedded FPGA (Xilinx), a microcontroller, and a reconfigurable Input/Output interface (NI CompactRIO).

Analog modification and uniformity tests of synstors

To examine the analog modification and uniformity of the circuit, the 64 synstors in the circuit were tuned to 1000 targeted analog values, w_t, evenly separated by $\Delta w_t = 59$ pS, by applying a train of paired 10-μs-wide x and z pulses concurrently with an amplitude of −4 V (or 4 V) on each synstor until their conductance values reached the targeted analog values closely.

Endurance tests of the synstors

The endurance testing of the synstors was performed by modification of their conductance to high (16 nS) and low (5 nS) conductance values by iterative application of paired 3-μs-wide x and z pulses concurrently with an amplitude of − 6 V (or 7 V). Endurance testing of the synstors was also conducted by adjusting their conductance to the maximum (60 nS) and minimum (0.6 nS) values through iterative application of paired 200-μs-wide x and z pulses concurrently with an amplitude of − 6 V (or 7 V).

Synstor test at different temperatures

The currents (I) through synstors were measured as a function of input voltage (x) using a Keithley 4200 semiconductor parameter analyzer. The synstors were tested at temperatures between 24° and 80°C. Conductance was adjusted to a target value by iteratively applying paired 3-μs-wide x and z pulses concurrently with amplitudes of −6 or 7 V.

Resistance tests of $WO_{2.8}$ reference electrodes

$WO_{2.8}$ thin-film resistors, with a thickness of 80 nm, a width of 40 μm, and a length of 100 μm, were fabricated on SiO_2 surface using the methods described in the synstor fabrication process. The current-voltage characteristics and resistance of the $WO_{2.8}$ resistor were measured using a Keithley 4200 semiconductor parameter analyzer over a temperature range of 80 to 320 K in a Lake Shore cryogenic probe station.

Nonvolatile memory tests of the synstors

Synstor conductance values were modified to different initial analog conductance values, $w(0)$, by applying paired positive or negative pulses, and their conductance values, w, were measured versus time, t, over 1.2×10^6 s at a temperature of 40° and 85°C, respectively.

Polarization-voltage (*P-V*) measurement on HfZrO films

We fabricated capacitors composed of a HfZrO film for its *P-V* measurement. A blanket thin film of 70-nm-thick W was sputter coated as a bottom electrode (BE) on a 300-nm-thick SiO_2 layer grown thermally on a silicon wafer. A 10-nm-thick HfZrO film was deposited on the BE via ALD as described in Materials and Methods about synstor fabrication. A 45-nm-thick W layer was then sputter deposited as a top electrode, and a 50-nm-thick platinum (Pt) was used to cap off the capacitors. Capacitors with a 30 μm–by–30 μm W top electrode patterned via photolithography and liftoff processes were annealed at 500°C.

Drone flying in a simulated environment

The experiments were performed by flying a drone in an environment (Fig. 5 and movie S1) simulated by running an AirSim program (Microsoft Co.) in a Dell computer with an Intel i9-12900 CPU and NVIDIA RTX 3060 Ti GPU. During the flight, wind randomly changed its direction and speed from 0 to 17.5 m/s (fig. S8). The positions of the drone and target were determined by a simulated global positioning system. To avoid collisions with obstacles such as mountains and trees in the environment, the depth profiles of the obstacles were detected by a simulated camera mounted on the

drone and analyzed to identify local flight target positions with obstacle clearance and minimal objective function $F = \frac{1}{2}\left(\mathbf{s}-\hat{\mathbf{s}}\right)^2$, where $\mathbf{s}-\hat{\mathbf{s}}$ as the deviations of the drone position ($\mathbf{s}$) from its target position ($\hat{\mathbf{s}}$) along upward, downward, forward, backward, left, right, clockwise, and anticlockwise (yaw) dimensions (fig. S7D).

Experiments to drive a drone by a synstor circuit

The conductance values in the matrix of the synstor circuit, $\mathbf{W}$, were set to random values before each learning experiments started (fig. S9). As shown in Fig. 5, figs. S7A and S8A, and movie S1, $\mathbf{s}-\hat{\mathbf{s}}$ was converted to voltage pulses, $\mathbf{x}$, with an amplitude of −3 or 4.2 V and a duration of 10 ns, which were input to the synstor circuit by the interface circuit (FPGA, Xilinx, Kintex-7). The firing rate of $\mathbf{x}$ pulses increased monotonically with increasing $\mathbf{s}-\hat{\mathbf{s}}$. $\mathbf{x}$ generated currents, $\mathbf{I}=\mathbf{W}\mathbf{x}$ (Eq. 1), via the synstor circuit. The currents, $\mathbf{I}$, flowed through the synstors to interface circuits and triggered the actuation pulses, $\mathbf{y}$, to drive the drone, and the voltage pulses, $\mathbf{z}$, applied on the output electrodes of the synstor circuit to modify the synstor conductance matrix, $\mathbf{W}$, by following the learning rule, $\dot{\mathbf{W}} = \alpha\,\mathbf{z}\otimes\mathbf{x}$ (Eq. 2). Neuron circuits were designed in our laboratory and fabricated in Taiwan Semiconductor Manufacturing Company to emulate the functions of biological neurons. When $I < I_{th} \approx 30$ nA, the threshold current of the neuron circuit, no actuation pulse was triggered. When $I_{th} \le I \le I_S \approx 60$ nA, the saturation current of the neuron circuit, the average firing rate of the actuation pulses increased monotonically with increasing I. When $I > I_S$, the average firing rate of the actuation pulses was saturated at ~14 Hz. The output pulses from the neuron circuits were converted to actuation signals, $\mathbf{y}$, by the interface circuit (FPGA, Xilinx, Kintex-7) to drive the drone (Fig. 5 and fig. S7A). The voltage pulses, $\mathbf{z}$, were triggered from the neuron circuits. The $\mathbf{z}$ pulses satisfied the conditions $\overline{z}_n = 0$ (Eq. 3) and $\overline{z_n y_n} \le 0$ (Eq. 4). When a y_n pulse was triggered at moment $t = t_n$ from the nth output neuron of the synstor circuit, a train of negative (or positive) z_n pulses were triggered at the nth (or nth complimentary) output electrodes within the time window $t_n < t < t_n + t_w$, and a train of positive (or negative) z_n pulses were triggered at the nth (or nth complimentary) output electrodes within the time window $t_n + \tau_+ < t < t_n + \tau_+ + t_w$, where $\tau_+ = 1180$ ms and $t_w = 40$ ms represents the duration of the time window of the pulse trains.

Experiments to navigate a drone by human operators

In the experiments with the drone driven by humans under the same environment of the synstor circuit experiments (Materials and Methods, Fig. 5, figs. S7B and S8B, and movie S1), 14 human operators without any prior knowledge of the drone and its control system visually received $\mathbf{s}_L$ signals displayed on a computer monitor and were instructed to drive the drone toward its local target position and avoid the collision with obstacles by minimizing the $\mathbf{s}-\hat{\mathbf{s}}$ values. The $\mathbf{s}-\hat{\mathbf{s}}$ signals were processed by the neurobiological circuits in the human brains, triggering actuation pulses $\mathbf{y}$ to drive the drone by pressing eight keys in a keyboard (fig. S8B). The firing rates of $\mathbf{y}$ pulses were proportional to the keystroke times.

Experiments to drive a drone by an ANN running on a computer

The experiments with the drone driven by a computer-based ANN were performed under the same environment as the synstor circuit and human experiments (Fig. 5, figs. S7C and S8C, and movie S1). Before the learning experiment started, the digital synaptic weight matrix, $\mathbf{W}$, in the ANN was also set to random values, the same as for the trials of the synstor circuit. The time required to execute learning function was significantly longer than that to execute the inference function during the flight (fig. S10F); thus, it is infeasible to execute the real-time learning on the computer, and the inference and learning are executed sequentially. The ANN running on a Dell computer (Intel i9-12900 CPU and NVIDIA RTX 3060 Ti GPU) received the $\mathbf{s}-\hat{\mathbf{s}}$ signals, converted $\mathbf{s}-\hat{\mathbf{s}}$ to input signals, $\mathbf{x}$, and induced output current $\mathbf{I}=\mathbf{W}(n)\,\mathbf{x}$, triggering actuation pulses, $\mathbf{y}$, to modify $\mathbf{s}_L$ at nth episode to drive the drone for ~30 s (Fig. 5C). After the nth flight episode ended, the saved data, $\mathbf{s}-\hat{\mathbf{s}}$, $\mathbf{y}$, and $\mathbf{W}(n)$ from the nth episode were sent back to the computer to execute a reinforcement learning function (*47*) (Supplementary Materials) for ~550 s to modify $\mathbf{W}(n)$ to $\mathbf{W}(n+1)$, which reset the ANN to drive the drone at the $(n+1)$th flight episode iteratively until the drone crashed into an obstacle or reached the final target. ANNs with (i) 8 neurons at its input layer, no hidden layer, and 9 neurons at its output layer interconnected by 72 synapses and (ii) 8 neurons at its input layer, 128 neurons at its hidden layer, and 9 neurons at its output layer interconnected by 2176 synapses were tested to drive the drone toward a local target position in the learning experiments with a learning rate of 10^{-8}, 2×10^{-8}, 5×10^{-8}, and 10^{-7}, respectively (fig. S10). The optimal ANN with no hidden layer and a learning rate of 5×10^{-8} had the shortest learning time (fig. S10I) and were then used in the learning experiments to drive the drone toward the final target.

Average learning time

In the learning processes of synstor circuits, humans, and ANN, the change rate of the objective function, $\dot{F}$, is a nonlinear function of F but can be best fitted by a linear dynamic model $\dot{F} = -\left(F-F_e\right)/T_L$ and its solution over the learning processes (Fig. 6)

$$F(t) = \left[F(0)-F_e\right] e^{-t/T_L} + F_e \tag{6}$$

where the fitting parameter T_L represents the average initial learning time, and F_e represents the quasiequilibrium objective function when $t \gg T_L$ and $d\overline{F}/dt \approx 0$.

Power consumptions of concurrent inference and learning by the synstor circuit

When voltage pulses were applied on a 8×8 crossbar synstor circuit, the average power consumption of the circuit (excluding the power consumptions of interface circuits), $P = \mathbf{I}\otimes\mathbf{x} = (\mathbf{w}\mathbf{x})\otimes\mathbf{x} \approx w_T\,V_a^2 D_p$, where w_T denotes the total conductance of the synstors in the circuit, V_a denotes the magnitude of pulses, and D_p denotes the average duty cycle of the pulses. During the concurrent signal processing and learning in the synstor circuit for the drone, $w_T \approx 10$ nS, $V_a = 4.2$ V, and $D_p = 0.014$; thus, $P \approx 158$ nW. On the basis of the circuit simulation, the total power consumption of the eight neuron circuits was ~0.78 nW.

Computing energy and area efficiency of the synstor circuit

A crossbar synstor circuit with an $M\times N$ synstors executes the inference algorithm with a computing speed of $2MNf_p$, which corresponds to MN

analog multiplications between **W** and **x**, and *MN* analog accumulations, performed at an analog signal input rate, f_i. The learning algorithm is executed at a computing speed of $4MNf_i$, which corresponds to $3MN$ analog outer products between α, **x**, and **z**, and *MN* modifications of **W**, also at the rate of f_i. The average computing speed for a synstor circuit with $M \times N$ synstors to concurrently execute the inference and learning algorithms in analog parallel mode is $V_c = 6MNf_i$. For $f_i = 50$ MHz, the computing speed of the 8×8 crossbar synstor circuit is $V_c = 1.92 \times 10^{10}$ OPS. The computing energy efficiency is calculated as $E_f = V_c / P \approx 1.2 \times 10^{17}$ OPS / W. With a synstor active area of approximately $S \approx 2 \times 10^{-4}$ mm^2, the average area efficiency of the 8×8 crossbar synstor circuit is $E_s = V_c / (MNS) \approx 1.5 \times 10^{12}$ OPS / mm^2.

Power consumptions of sequential inference and learning by the computer

According to analysis from Python toolkits "keras_flops" and "pyperf," the speeds for sequentially executing the inference and learning programs on the computer were estimated to be 3.9 kilo floating-point operations per s and 2.0 giga floating-point operations per s, respectively. With a computing energy efficiency of 3.1 giga floating-point operations per s (*54*), the power consumption for sequentially executing the inference and learning programs on the computer was 12 μW and 6.3 W, respectively. The aggregate power consumption of the ANN for sequential inference and learning is 6.3 W (Fig. 6).

Computer-aided device and circuit simulation

On the basis of the properties of synstors and their circuits, we have designed and simulated synstors and their circuits by SPICE (Simulation Program with Integrated Circuit Emphasis) simulators (SPECTRE from Cadence and HSPICE from Synopsys) (*35*). The simulator performed numerical calculations of the device physics by solving Poisson's equation describing the electrostatics and drift-diffusion carrier transport under a set of boundary conditions defined by the device structure. Quasistationary simulations were conducted under various voltage biases on the input/output electrodes of the synstors with respect to the grounded reference electrodes. The band diagrams of the synstors were extracted from the simulations, and the electronic properties of the synstors were analyzed by the simulations. According to the Technology Computer-Aided Design simulation, when the synstor channel length and the reference electrode length are scaled down to 100 and 40 nm, respectively, the synstor still functions properly for inference and learning (fig. S12). We have designed and simulated a synstor circuit based on a GlobalFoundries 28-nm ferroelectric process, which has an average synstor conductance $\langle w \rangle \approx 0.2$ nS, $R_e \approx 0.54$ ohms; thus, $M, N \lesssim 10^4$, i.e., a single crossbar synstor circuit can be scaled up to $M, N = 10^4$ with $M \cdot N = 10^8$ synstors.

Sequential inference and reinforce learning executed in the ANN

The sequential inference (flight) and reinforcement learning functions (*47*) executed in the ANN is briefly described mathematically as follows:

Initialize random synaptic weight matrix $\mathbf{W}(0)$ in the ANN.

Loop for episodes $n = 1, 2, \ldots, N_T$ until the drone reaches the final target or crashes into an obstacle.

In the *n*th inference (flight) episode that lasted ~30 s, generate data $\mathbf{s} - \hat{\mathbf{s}}$, $\mathbf{y}$, and $\mathbf{W}(n)$ by following the inference function $f\left[y(t) \,|\, s_L(t), W(n)\right]$ in the ANN at discrete time steps $t = 0, 1, \ldots, N_D$ at the frequency of 12.5 kHz with input signals, $\mathbf{s} - \hat{\mathbf{s}}$, as the deviations of the drone position from the local target $\mathbf{W}(n)$ as the ANN synaptic weight matrixes in the *n*th flight episode and $\mathbf{y}(t)$ as actuation pulses to drive the drone.

After the *n*th inference (flight) episode ends, start the *n*th learning episode.

In the *n*th learning episode, loop for discrete time steps $t = 0, 1, \ldots, N_D, \Gamma(t+1) = \Gamma(t) + r_L \mu^t (G(t) - b) \nabla_\Gamma \ln\left\{f\left[y(t) \,|\, \left(s - \hat{s}\right), \Gamma_k\right]\right\}$, where $\Gamma(0) = \mathbf{W}(n)$, learning rate $r_L > 0$, discount factor $\mu > 0$, $G(t) = \sum_{j=t+1}^{N_D} \mu^{j-t-1} R(j)$, baseline $b = \sum_t G(t) / N_D$, and reward $R(j)$.

Update $\mathbf{W}(n+1) = \Gamma\left(N_D\right)$.

Supplementary Materials

The PDF file includes:

Figs. S1 to S12

Legend for movie S1

Other Supplementary Material for this manuscript includes the following:

Movie S1

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